Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-23, leaving claims 24-54 for examination as follows:

Listing of Claims:

1-23. (Cancelled)

24. (Original) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array including a plurality of word lines;

a voltage switching circuit, comprising,

an active voltage reference adapted to receive a mode signal, the active voltage reference operable responsive to the mode signal going active to generate a first reference voltage and operable responsive to the mode signal going inactive to terminate generation of the first reference voltage;

a standby voltage reference operable to generate a second reference voltage;

a charge pump operable to generate a row drive voltage having a value that is a function of a reference voltage;

a plurality of row drivers, each row driver being coupled to the address decoder to receive a corresponding decoded address signal and including an output coupled to a corresponding word line of the memory-cell array, and coupled to the charge pump

to receive the row drive voltage, the row driver applying the row drive voltage on the word line responsive to the decoded address signal being active;

a multiplexer coupled to the active and standby voltage references to receive the first and second voltage references, respectively, and being coupled to the charge pump, the multiplexer applying the first reference voltage to the charge pump responsive to a selection signal going active, and applying the second reference voltage to the charge pump responsive to the selection signal going inactive;

a delay circuit coupled to the multiplexer and adapted to receive the mode signal, the delay circuit operable responsive to the mode signal going active to drive the selection signal active a delay time after the mode signal goes active, and operable responsive to the mode signal going inactive to drive the selection signal inactive without the delay time.

25. (Original) The memory device of claim 24 wherein the active and standby voltage references each comprise a bandgap voltage reference.

26. (Original) The memory device of claim 24 wherein the memory device comprises a flash memory.

27. (Original) The memory device of claim 24 wherein the mode signal comprises a chip enable signal applied on the control bus.

28. (Original) The memory device of claim 27 wherein the chip enable signal goes active to place the memory device in an active mode of operation and goes inactive to place the memory device in a standby mode of operation.

29. (Original) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array including a plurality of word lines;

a voltage switching circuit, comprising,

an active voltage reference adapted to receive a mode signal, the active voltage reference operable responsive to the mode signal going active to generate a first reference voltage and operable responsive to the mode signal going inactive to terminate generation of the first reference voltage;

a standby voltage reference operable to generate a second reference voltage;

a charge pump operable to generate a row drive voltage having a value that is a function of a reference voltage;

a plurality of row drivers, each row driver being coupled to the address decoder to receive a corresponding decoded address signal and including an output coupled to a corresponding word line of the memory-cell array, and coupled to the charge pump to receive the row drive voltage, the row driver applying the row drive voltage on the word line responsive to the decoded address signal being active;

a multiplexer coupled to the active and standby voltage references to receive the first and second voltage references, respectively, and being coupled to the charge pump, the multiplexer applying the first reference voltage to the charge pump responsive to a selection signal going active, and applying the second reference voltage to the charge pump responsive to the selection signal going inactive;

a delay circuit coupled to the multiplexer and adapted to receive the mode signal, the delay circuit operable responsive to the mode signal going active to drive the selection signal active a delay time after the mode signal goes active, and operable responsive to the mode signal going inactive to drive the selection signal inactive without the delay time.

30. (Original) The computer system of claim 29 wherein the active and standby voltage references each comprise a bandgap voltage reference.

31. (Original) The computer system of claim 29 wherein the memory device comprises a flash memory.

32. (Original) The computer system of claim 29 wherein the mode signal comprises a chip enable signal applied on the control bus.

33. (Original) The computer system of claim 32 wherein the chip enable signal goes active to place the memory device in an active mode of operation and goes inactive to place the memory device in a standby mode of operation.

34. (Original) A method of operating a memory, the method comprising:

detecting an active mode of operation of the memory;

during the active mode of operation,

generating a first reference voltage;

generating a word line drive voltage using the first reference voltage;

receiving addresses corresponding to memory cells to be accessed; and

applying the word line drive voltage to the word line of addressed memory cells to access the memory cells in the corresponding row; and

detecting a standby mode of operation; and

during the standby mode of operation,

terminating generation of the first reference voltage;

generating a second reference voltage; and

generating the word line drive voltage using the second reference voltage.

35. (Original) The method of claim 34 wherein detecting the active and standby modes of operation comprises detecting a signal applied to the flash memory on the control bus.

36. (Original) The method of claim 35 wherein the signal comprises a chip enable signal.

37. (Original) The method of claim 34 wherein generating the first reference voltage consumes more power than generating the second reference voltage.

38. (Original) A method of operating a memory, the method comprising:

detecting an active mode of operation of the memory;

during the active mode of operation,

generating a first reference voltage that consumes a first amount of power in generating the first reference voltage;

generating a word line drive voltage using the first reference voltage;

generating a second reference voltage that consumes a second amount of power in generating the second reference voltage, the second amount of power being less than the first amount of power;

detecting a standby mode of operation of the memory; and

during the standby mode,

terminating generation of the first reference voltage; and

generating the word line drive voltage using the second reference voltage.

39. (Original) The method of claim 38 wherein detecting the active and standby modes of operation comprises detecting a signal applied to the flash memory on the control bus.

40. (Original) The method of claim 39 wherein the signal comprises a chip enable signal.

41. (Original) The method of claim 38 wherein the first reference voltage has a value that is more precise and stable relative to the value of the second reference voltage.

42. (Original) The method of claim 38 wherein generating a second reference voltage comprises generating the second reference voltage during the active and standby modes of operation.

43. (Original) A method of operating a memory, the method comprising:

detecting a standby mode of operation of the memory;

generating a first reference voltage;

generating a word line drive voltage using the first reference voltage;

detecting an active mode of operation of the memory;

during the active mode of operation,

generating a second reference voltage;

generating the word line drive voltage using the first reference voltage; and

generating the word line drive voltage using the second reference voltage.

44. (Original) The method of claim 43 wherein during the active mode the generation of the word line drive voltage using the first reference voltage comprises generating the word line drive voltage using the first reference voltage for a delay time, the delay time defining an interval after the detection of the active mode, and wherein during the active mode the generation of the word line drive voltage using the second reference voltage comprises generating the word line drive voltage using the second reference voltage after the delay time.

45. (Original) The method of claim 43 wherein during the active mode the generation of the word line drive voltage using the first reference voltage comprises generating the word line drive voltage using the first reference voltage for a predetermined number of data transfer operations after the start of the active mode, and wherein during the active mode the generation of the word line drive voltage using the second reference voltage comprises generating the word line drive voltage using the second reference voltage after the predetermined number of data transfer operations.

46. (Original) The method of claim 43 wherein detecting the active and standby modes of operation comprises detecting a signal applied to the flash memory on the control bus.

47. (Original) The method of claim 46 wherein the signal comprises a chip enable signal.

48. (Original) The method of claim 43 wherein the second reference voltage has a value that is more precise and stable relative to the value of the first reference voltage.

49. (Original) A method of operating a memory, the method comprising:

generating a first reference voltage;

detecting an active mode of operation of the memory;

upon detection of the active mode,

commencing the charging of a node to develop a second reference voltage on the node, the second reference voltage having desired value;

generating the word line drive voltage using the first reference voltage while the node is charging the second reference voltage to the desired value; and

generating the word line drive voltage using the second reference voltage once the second reference voltage on the node has been charged to the desired value;

detecting a standby mode of operation of the memory;

upon detection of the standby mode,

terminating the charging of the node; and

generating the word line drive voltage using the first reference voltage.

50. (Original) The method of claim 49 wherein generating the word line drive voltage using the first reference voltage while the node is charging the second reference voltage to the desired value comprises generating the word line drive voltage using the first reference voltage for a delay time, the delay time defining an interval after the active mode is detected, and wherein generating the word line drive voltage using the second reference voltage once the node has charged the second reference voltage to the desired value comprises generating the word line drive voltage using the second reference voltage after the delay time.

51. (Original) The method of claim 49 wherein generating the word line drive voltage using the first reference voltage while the node is charging the second reference voltage to the desired value comprises generating the word line drive voltage using the first reference voltage for a predetermined number of data transfer commands applied to the memory after the active mode is detected, and wherein generating the word line drive voltage using the second

reference voltage once the node has charged the second reference voltage to the desired value comprises generating the word line drive voltage using the second reference voltage after the predetermined number of data transfer commands have been applied.

52. (Original) The method of claim 49 wherein detecting the active and standby modes of operation comprises detecting a signal applied to the flash memory on the control bus.

53. (Original) The method of claim 52 wherein the signal comprises a chip enable signal.

54. (Original) The method of claim 49 wherein the second reference voltage has a value that is more precise and stable relative to the value of the first reference voltage.